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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,029	09/24/2003	Mark Templeton	ARTCP047	7834

25920 7590 04/07/2005

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,029	TEMPLETON ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3 and 14-19* is/are allowed.

6)☒ Claim(s) *4,5,10 and 11* is/are rejected.

7)☒ Claim(s) *6-9,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/24/2003 and 03/01/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to applicant's Amendment and Remarks filed on 03/01/2005 regarding application 10/671,029 filed on 09/24/2003. Claims 1 – 19 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 7, before "different standard cell variants" insert **—plurality of—**.
Claim 2, line 7, before "different standard cell variants" insert **—plurality of—**.
Claim 2, line 7, change "problem;" to **—problem, wherein the plurality of different variants are designed to at least address the manufacturing problems of poor contact formation, contact alignment, metal line spacing and metal line direction changes; —**.
Claim 2, line 12 – 14, delete **—wherein the variants are designed to at least address the manufacturing problems of poor contact formation, contact alignment, metal line spacing and metal line direction changes; —**.
Claim 3, line 7, before "different standard cell variants" insert **—plurality of—**.
Claim 4, line 7, before "design variant" delete **—the—**.
Claim 9, line 2, before "manufacturing" delete **—the—**.
Claim 9, line 2, change "the particular valiant" to **—a particular variant—**.
Claim 14, line 1, before "manufacturability" delete **—the—**.
Claim 14, line 4, before "variant designs" insert **—plurality of—**.
Claim 14, line 7, change "the design" to **—the proposed IC design—**.
Claim 16, line 1, before "manufacturability" delete **—the—**.
Claim 16, line 4, before "variant designs" insert **—plurality of—**.
Claim 16, line 7, change "the design" to **—the proposed IC design—**.
Claim 16, line 10, before "variant designs" insert **—plurality of—**.
Claim 19, line 1, before "manufacturability" delete **—the—**.
Claim 19, line 4, before "variant designs" insert **—plurality of—**.
Claim 19, line 7, change "the design" to **—the proposed IC design—**.
Claim 19, line 9, before "variant designs" insert **—plurality of—**.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 4, 5, 10 and 11 are rejected under 35 U.S.C. 102(e) as being unpatentable over U.S. Patent Application Publication No. 2003/0188268 A1 to *Konstadinidis et al.*

5. As to Claim 4, *Konstadinidis et al.* teach the following subject matter:

- Optimizing timing constraint of an integrated circuit design using multiple *standard cells* (i.e., *standard components*) – [abstract; Paragraph 0005; 0006];
- Designing different threshold V_t gate instances (i.e., a plurality of variants) of *standard cells* (*standard components*) – [abstract; Paragraph 0005; 0006];
- Prioritizing each threshold V_t gate instance (i.e., design variant) based on timing variable – [abstract; Paragraph 0005]; Notice that the prioritizing is performed to provide rating of each threshold V_t gate instance based on timing;
- Selectively substituting (low) V_t gate whose timing priority most closely matches timing constraints (i.e., designer's criteria) on all timing paths in the integrated circuit design – [abstract; Paragraph 0005].

6. As to Claim 10, threshold voltage V_t addresses controlling threshold voltage level of transistors, which is a manufacturing problem to be solved, on all timing paths in the integrated circuit design – [Paragraph 0005]

7. As to Claims 5 and 11, *Konstadinidis et al.* teach standard cells (standard components) comprise logic gates or flops – [Paragraph 0006]. Notice that logic gates and/or flops are standard logic cells.

Reasons for Allowance

8. Claims 1 – 3 and 14 – 19 are allowed. Claims 6 – 9, 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the logic verification method and apparatus of:

- A method for improving yield of an integrated circuit through a manufacturing environment, the method comprising the step of *designing a plurality of different variant for standard cells in a library, each of the plurality of different standard cell variants addressing a different manufacturing problem* in combination with other limitations as recited in independent **Claim 1**, **Claim 2** and **Claim 3**, respectively;
- A system for improving manufacturability of an integrated circuit, the system comprising *a library comprised of a plurality of variant designs for standard components of the integrated circuit, each of the variant designs compensating for at least a known manufacturing problem* in combination with other limitations as recited in independent **Claim 14**, **Claim 16** and **Claim 19**, respectively.
- A method for allowing an integrated circuit designer to optimize an integrated circuit design, the method comprising the steps of *designing a plurality of variants of standard components*, *rating each design variant on at least one variable* and *selecting the design variant whose rating most closely matches designer's criteria for use in the integrated circuit design* *wherein the standard components comprise input/output cells* as recited in **Claim 6**;
- A method for allowing an integrated circuit designer to optimize an integrated circuit design, the method comprising the steps of *designing a plurality of variants of standard components*, *rating each design variant on at least one variable* and *selecting the design variant whose rating most closely matches designer's criteria for use in the integrated circuit design* *wherein the standard components*

comprise memory core cells or entire memory blocks including core cells as recited in **Claim 7**;

- A method for allowing an integrated circuit designer to optimize an integrated circuit design, the method comprising the steps of *designing a plurality of variants of standard components*, *rating each design variant on at least one variable* and *selecting the design variant whose rating most closely matches designer's criteria for use in the integrated circuit design* *wherein the standard components perform at least an analog function including one of at least phase locked loops and analog-to-digital converters* as recited in **Claim 8**;
- A method for allowing an integrated circuit designer to optimize an integrated circuit design, the method comprising the steps of *designing a plurality of variants of standard components*, *rating each design variant on at least one variable* and *selecting the design variant whose rating most closely matches designer's criteria for use in the integrated circuit design* *wherein each of the standard components and its variants are characterized to indicate manufacturing yield of a particular variant* as recited in **Claim 9**;
- The method of Claim 11 wherein *the variants of standard logic cells have each been assigned a rating that indicates its manufacturability in at least a manufacturing environment* as recited in **Claim 12**.

Response to Amendment and Remarks

9. Applicants' amendment and remarks filed on 03/01/2005 have been reviewed. Applicants' arguments have been fully considered; they are persuasive. Claims 1 – 3 and 14 – 19 are allowed. Claims 6 – 9, 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, due new grounds of rejections have been founded, Claims 4, 5 10 and 11 are rejected. Detailed responses are provided in this Office Action given above.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun J. Lin
Patent Examiner
Art Unit 2825
April 5, 2005